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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,936	FARNWORTH, WARREN M.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 29-55 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 29-55 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 10 July 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/10/03; 2/26/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 29-33, 35, 36, 40, 41, 49-51, and 53 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,218,281 to Watanabe et al. (cited by applicant).

Regarding claims 29, 36, 49, and 50 Watanabe discloses fabricating a semiconductor component by: providing a die (30/40) comprising a circuit side and a plurality of die contacts in electrical communication with an IC (column 10, lines 33-45) on the circuit (32/42) having a first pattern (see figure 6, 10); forming a polymer layer (43) on the circuit side (figures 6 and 10); forming a plurality of redistribution conductors (44, 47a, 47b/33) on the polymer layer in electrical communication with the die contacts (figure 10); and forming a plurality of bonding pads (formed from 44, 47a, 47b/31) on the polymer layer in electrical communication with the conductors (figure 10) and having a second pattern (figure 6; figure 10), each bonding pad comprising: a conductive layer (44); a barrier/adhesion layer (47a), and a non-oxidizing layer (47b). Since the thickness of the layers must directly affect the electrical properties of the

conductors, it is implicit that controlling/selecting a thickness of the barrier/adhesion layer will adjust the electrical characteristic.

Regarding claims 31-32 and 41, Watanabe discloses that a non-oxidizing layer comprising Pd or Au covers the bonding pad and the conductor (column 14, lines 1-6), and that the metal barrier layer comprises Cu (column 14, lines 1-5).

Regarding claims 33 and 53, Watanabe discloses forming stud bumps (63 and 66) on the bonding pads (figures 9D and 10).

Regarding claims 35 and 51, Watanabe discloses a second polymer (60) on the conductors with openings aligned with the bonding pads (column 13, lines 20-30; figure 10).

Regarding claim 40, Watanabe discloses that the polymer layer comprises polyimide (column 10, lines 46-50).

3. Claims 29-33, 35, 36, 40, 41, 49-51, and 53 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,455,408 to Hwang et al. (cited by applicant).

Regarding claims 29, 36, 49, and 50, Hwang discloses fabricating a semiconductor component by: providing a die (52) comprising a circuit side with a plurality of ICs (column 1, lines 34-40) in electrical communication with a plurality of die contacts (54; also see figures. 2 and 3); the die contacts having a first pattern (figure 2); forming a polymer layer (58) on the die (figures 13 and 17); forming a redistribution conductor (60) made of copper (column 4, lines 10-15) on the polymer layer comprising a conductive layer (60) in electrical communication with the die contact; and forming a bonding pad (region under (80) in figure 17) comprising the conductive layer, a barrier layer (64) covering the conductive layer (figures 13 and 17), and a

non-oxidizing layer (70; see column 5, lines 10-20) the bonding layer having a second pattern (figure 3). Since the thickness of the layers must directly affect the electrical properties of the conductors, it is implicit that controlling/selecting a thickness of the barrier/adhesion layer will adjust the electrical characteristic.

Regarding claims 30 and 32, Hwang discloses a non-oxidizing metal layer (70) comprising Palladium (column 5, lines 10-20) and covering the bonding pad and conductor (figures 13 and 17).

Regarding claims 31 and 41, Hwang discloses that the barrier/adhesion layer comprises Ni or Cu (column 4, lines 37-43).

Regarding claims 35 and 51, Hwang discloses a second polymer layer (74) covering the conductor and polymer layer but leaving the bonding pad exposed (figure 17).

Regarding claim 40, Hwang discloses that the polymer comprises PBO, BCB or polyimide (column 3, line 65 – column 4, line 2).

Regarding claims 33 and 53, Hwang discloses a stud bump (80) bonded to each bonding pad (figure 17).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 42, 43, 45, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang et al. in view of U.S. Patent No. 6,197,613 to Kung et al.

Regarding claims 42 and 46, Hwang discloses providing a semiconductor wafer substrate (52; also see column 3, lines 50-60) comprising a semiconductor die having a plurality of contacts (54; figures 2, 3, and 8); forming a polymer layer (58) on the die; forming a plurality of conductors (60) on the polymer layer in electrical communication with the die contact (figure 9), the conductors comprising bonding pads (exposed region 76 in figure 16) having a different pattern than the die contacts (figures 2 and 3); forming a barrier/adhesion layer (64; Cu or Ni act as a barrier layer) on the conductors and bonding pads (figure 16); forming a non-oxidizing layer (70; column 5, lines 14-20) on the barrier/adhesion layer (figure 16); and singulating the die from the substrate (column 1, lines 34-48).

Hwang fails to disclose that a metal bump is formed on the die contact, and that the polymer layer and metal bumps are planarized to the same surface.

Kung discloses a redistribution structure in which a metal bump (68) is formed on the die contact (54), and then the metal bump and a polymer layer (70; column 8, lines 30-35; figures 2G-2H).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the redistribution structure of Hwang, such that a metal bump planarized with a polymer layer is provided, as suggested by Kung. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a metal bump on the die contact, and then planarize the bump and polymer layer before depositing the redistribution structure, because such an arrangement minimizes processing-induced stresses and improves the

reliability of the chip (see Kung, column 3, lines 45-57; column 4, lines 1-27; column 9, lines 1-15).

Regarding claim 43, Hwang discloses stud bumps (80) bonded to each bonding pad (figure 17).

Regarding claim 45, Hwang discloses a second polymer layer (74) covering the conductor and polymer layer but leaving the bonding pad exposed (figure 17).

6. Claims 42, 43, 45, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. in view of Kung et al.

Regarding claims 42 and 46, Watanabe discloses: providing a semiconductor wafer die substrate (30/40; column 10, lines 32-40) comprising a plurality of die contacts; forming a polymer layer (43) on the die (figures 6 and 10); forming a plurality of redistribution conductors (44, 47a, 47b/33) on the polymer layer in electrical communication with the die contacts (figure 10); and forming a plurality of bonding pads (formed from 44, 47a, 47b/31) on the polymer layer in electrical communication with the conductors (figure 10) and having a different pattern than the die contacts (figures 6 and 10); forming a barrier/adhesion layer (47a), forming a non-oxidizing layer (47b), and singulating the die (figure 6 shows a singulated die).

Kung discloses a redistribution structure in which a metal bump (68) is formed on the die contact (54), and then the metal bump and a polymer layer (70; column 8, lines 30-35; figures 2G-2H).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the redistribution structure of Watanabe, such that a metal bump planarized

with a polymer layer is provided, as suggested by Kung. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a metal bump on the die contact, and then planarize the bump and polymer layer before depositing the redistribution structure, because such an arrangement minimizes processing-induced stresses and improves the reliability of the chip (see Kung, column 3, lines 45-57; column 4, lines 1-27; column 9, lines 1-15).

Regarding claim 43, Watanabe discloses forming stud bumps (63 and 66) on the bonding pads (figures 9D and 10).

Regarding claim 45, Watanabe discloses a second polymer (60) on the conductors with openings aligned with the bonding pads (column 13, lines 20-30; figure 10).

7. Claims 34, 54, and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al in view of U.S. Patent No. 6,335,104 to Sambucetti et al. (cited by applicant).

Watanabe discloses that it is advantageous to provide pads for wirebonding, such that the chip is compatible with both wirebonding and flip chip bonding (see column 5, lines 15-25; column 10, lines 10-30), but fails to specify that the bonding pad formed from the redistribution layer is used for wirebonding.

Sambucetti discloses that the same bonding pad with a structure substantially similar to that of Watanabe (see Sambucetti, column 5, line 60 – column 6, line 15) can be used for both flip chip bonding using a solder ball/bump or for wirebonding (figures 1 and 2; column 2, lines 20-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the package of Watanabe such that the bonding pad is connected by a wire bond, as is suggested by Sambucetti. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a wire bond or provide a stud bump that can be used for either wirebonding or flip chip bonding, in order to have compatibility with mounting substrates or wiring boards designed for wire-bonding rather than flip chip bonding and in order to generally increase the versatility of the chip. Since wire bonding and stud-bump/flip chip bonding are widely known and used in the art, and since Sambucetti shows that the same bonding pad structure could be used equivalently and analogously for either a wirebond or a stud bump, it is well within the purview of a person having ordinary skill in the art to apply a wirebond to the bonding pad of Watanabe.

8. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. in view of Kung et al. as applied to claim 42 above, and further in view of Sambucetti et al.

Watanabe discloses that it is advantageous to provide pads for wirebonding, such that the chip is compatible with both wirebonding and flip chip bonding (see column 5, lines 15-25; column 10, lines 10-30), but fails to specify that the bonding pad formed from the redistribution layer is used for wirebonding.

Sambucetti discloses that the same bonding pad with a structure substantially similar to that of Watanabe (see Sambucetti, column 5, line 60 – column 6, line 15) can be used for both flip chip bonding using a solder ball/bump or for wirebonding (figures 1 and 2; column 2, lines 20-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the package of Watanabe as modified by Kung such that the bonding pad is connected by a wire bond, as is suggested by Sambucetti. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a wire bond or provide a stud bump that can be used for either wirebonding or flip chip bonding, in order to have compatibility with mounting substrates or wiring boards designed for wire-bonding rather than flip chip bonding and in order to generally increase the versatility of the chip. Since wire bonding and stud-bump/flip chip bonding are widely known and used in the art, and since Sambucetti shows that the same bonding pad structure could be used equivalently and analogously for either a wirebond or a stud bump, it is well within the purview of a person having ordinary skill in the art to apply a wirebond to the bonding pad of Watanabe.

9. Claim 37 is rejected under 35 U.S.C. 103(a) as being obvious over Hwang et al. in view of U.S. Patent No. 6,396,148 to Eichelberger et al. (cited by applicant).

Hwang fails to disclose that the conductor and bonding pads are formed by electrolessly deposition.

Eichelberger discloses that a metal interconnect is advantageously formed over a die contact pad by using electroless deposition (see column 3, lines 12-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the first metal layer/bonding pad of Hwang is made using electroless deposition, as suggested by Eichelberger. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use electroless deposition for providing the first

conductor, because electroless deposition provides strong adherence to the die contact, is significantly cheaper than other deposition processes, such as sputtering, allows for enhanced stress relief, and greatly simplifies the fabrication process (see Eichelberger, column 3, lines 12-28).

10. Claims 38, 39, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang et al in view of U.S. Patent No. 5,910,644 to Goodman et al. (cited by applicant).

Regarding claims 38 and 39, Hwang discloses that the barrier and non-oxidizing layers are electrolessly deposited.

Goodman discloses electrolessly (column 5, lines 54-55) plating a nickel layer, palladium layer, and then a gold layer on top of a copper interconnect in order to form a bonding pad suitable for solder ball or wirebond formation (see column 3, lines 10-40; column 5, line 30 – column 6, line 30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the barrier/adhesion and non-oxidizing layer deposition method of Hwang, such that electroless deposition of Ni, Pd, and Au is used, as suggested by Goodman. The rationale is as follows: A person having ordinary skill in the art would have been motivated to electrolessly plate a nickel barrier layer, followed by a palladium or gold non-oxidizing layer, because by electrolessly plating, a high quality, dense, low porosity, highly adherent film (see Goodman, column 5, lines 54-67) ideal for both wire-bonding and solder bump bonding (see Goodman, column 3, lines 10-20) can be cheaply formed (Goodman, column 5, lines 60-65).

Regarding claim 52, Hwang fails to teach that the non-oxidizing layer completely seals the conductors and bonding pads.

Goodman teaches that it is advantageous to coat a copper terminal layer (33) with nickel and gold (a non-oxidizing layer), such that the nickel completely covers the copper and the gold completely covers the nickel (see figure 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the redistribution terminal of Hwang, such that the metal layer completely covers (i.e. covers the edges of) the conductive layer, as suggested by Goodman. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a metal layer which covers the edges of the conductive layer, because Goodman shows that the nickel acts as a diffusion barrier for the copper, and thus completely blocks diffusion from the copper into the IC, and helps provide a robust surface ideal for wirebonding or soldering (Goodman, column 3, lines 10-30).

11. Claims 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang et al. in view of Kung et al. as applied to claim 42 above, and further in view of Goodman et al.

Hwang discloses that the barrier and non-oxidizing layers are electrolessly deposited.

Goodman discloses electrolessly (column 5, lines 54-55) plating a nickel layer, palladium layer, and then a gold layer on top of a copper interconnect in order to form a bonding pad suitable for solder ball or wirebond formation (see column 3, lines 10-40; column 5, line 30 – column 6, line 30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the barrier/adhesion and non-oxidizing layer deposition method of Hwang, such that electroless deposition of Ni, Pd, and Au is used, as suggested by Goodman. The rationale is as follows: A person having ordinary skill in the art would have been motivated to electrolessly plate a nickel barrier layer, followed by a palladium or gold non-oxidizing layer, because by electrolessly plating, a high quality, dense, low porosity, highly adherent film (see Goodman, column 5, lines 54-67) ideal for both wire-bonding and solder bump bonding (see Goodman, column 3, lines 10-20) can be cheaply formed (Goodman, column 5, lines 60-65).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,586,273 to Aiba et al. discloses an electrolessly deposited Ni/Au barrier layer disposed on a redistribution layer.

U.S. Patent Publication No.2001/0031548 to Elenius et al. discloses a 3-layer redistribution/barrier layer structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
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jmd

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